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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of: Callway, et al.	Examiner: C. Harrison
Application No.: 09/213,748	Group Art Unit: 2672
Filed: December 17, 1998	Our File No.: 00100.98.1319
For: METHOD AND APPARATUS FOR INDEPENDENT VIDEO AND GRAPHICS SCALING IN A VIDEO GRAPHICS SYSTEM	Docket No.: 0100.01319

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I hereby certify that these papers are being deposited with the United States Postal Service by Express Mail, postage pre-paid, on this date October 29, 2005, in an envelope addressed to: MAIL STOP APPEAL BRIEF - PATENTS, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

William J. Voller III — October 29, 2005 (Date)

TRANSMITTAL OF APPELLANT'S REPLY BRIEF PURSUANT TO 37 C.F.R. § 41.41

Transmitted herewith is the Appellant's Reply Brief pursuant to 37 C.F.R. § 41.41 in response to the Examiner's Answer mailed August 29, 2005 with respect to the Notice of Appeal filed on January 28, 2005 in the above-identified application.

Pursuant to 37 C.F.R. § 41.20(b)(2), the fee for filing the Reply Brief is $500.00 for a large entity. Authorization is hereby made to charge the amount of $500.00 to Deposit Account No. 50-0441. The Commissioner is also authorized to charge any additional fees required by this paper or credit any overpayment thereof to Deposit Account No. 50-0441. A duplicate of this paper is attached.

Respectfully submitted,

Date: October 29, 2005

By: _____
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APPELLANT'S REPLY BRIEF PURSUANT TO 37 C.F.R. § 41.41

Dear Sir:

Appellant submits this brief in response to the Examiner's Answer mailed August 29, 2005, in the above-identified application.

I. Real Party in Interest

Appellant respectfully incorporates Section I from the Appellant's Appeal Brief filed March 25, 2005.

II. Related Appeals and Interferences

In the Examiner's Answer, the Examiner indicated that Appellant's Appeal Brief filed March 25, 2005 did "not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal." (Examiner's Brief at 2.) The Examiner further indicated that it was "presumed that there are none" and that the "Board . . . may exercise its discretion to require an explicit statement as to the existence of any related appeals and interferences." (Examiner's Brief at 2.) As a point of clarification, Appellant expressly advised the Board of Patent Appeals and Interferences in its Appeal Brief filed March 25, 2005 that "[a]s presently advised, there are no related Appeals or Interferences filed, pending, or decided." (Appeal Brief at 1). Appellant respectfully repeats this statement in the present Reply Brief.

III. Status of Claims

Appellant respectfully incorporates Section III from the Appellant's Appeal Brief filed March 25, 2005.

Appellant thanks the Examiner for the statement that Appellant's arguments with respect to claims 15 and 16 are persuasive. (Examiner's Answer at 11.) Accordingly, the rejection with respect to claims 15 and 16 have been withdrawn by the Examiner in view of Appellant's Brief. (Examiner's Answer at 11.)

In summary, claims 1 and 5 have been cancelled and claims 15-16 and 31-37 are allowed. Claims 12-13 and 24-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Lastly, Claims 2-4, 6-11, 14, 17-23, 26-30 and 38 are currently rejected under 35 U.S.C. § 103(a). A copy of presently appealed claims 2-4, 6-14, 17-30 and 38 is attached in Appendix A below. Appellant respectfully submits that claims 2, 6, 8, and 10-11 stand or fall together with dependent claims 3, 7, 9, 14, 17 and 19 and independent claim 4. Similarly, Appellant respectfully submits that claims 21 and 23 stand or fall together with dependent claims 22 and 26-28 and independent claim 20. Claim 30 stands alone. Claim 38 stands alone. Claim 29 stands together with claim 18. Claims 24 and 25 stand together with claims 12 and 13, respectively.

IV. Status of Amendments

Appellant respectfully incorporates Section IV from the Appellant's Appeal Brief filed March 25, 2005. The claims listed in Appendix A reflect the presently appealed claims as they stood at the time the Final Office Action was mailed on August 25, 2004.

V. Summary of Claimed Subject Matter

Appellant respectfully incorporates Section V from the Appellant's Appeal Brief filed March 25, 2005.

VI. Brief Summary of the Prior Art References

Appellant respectfully incorporates Section VI from the Appellant's Appeal Brief filed March 25, 2005.

VII. Grounds of Rejection to be Reviewed on Appeal

The first issue on appeal is whether claims 2-4, 6-11, 14, 17-23, 26-30 and 38 are patentable under 35 U.S.C. § 103(a) in view of Fujimoto and further in view of Porter.

The second issue on appeal is whether claims 12-13 and 24-25 are patentable over the prior art reference cited.

VIII. Response to Examiner's Answer

Appellant respectfully reasserts its positions in its Appeal Brief filed March 25, 2005 and in addition, responds to the Examiner's Answer with the following brief comments.

The Examiner states that "Fujimoto teaches storing video and graphics together in a DVD memory that provides the stored video and graphics to a system for independent processing that results in the video and graphics being mixed and displayed." (Examiner's Answer at 4, emphasis added.) At another point, the Examiner concludes that "[t]hus, Fujimoto and Porter both teach combining the video and graphics data for storing in a single memory that is used as a source for providing the stored data to a system for independent processing before recombining and displaying the blended data." (Examiner's Answer at 5, emphasis added.)

However, the DVD operation of Fujimoto is described therein as merely reading pre-stored data from a DVD-ROM. (*See e.g.*, Fujimoto, col. 5, ll. 7-36; col. 11, ll. 16-41; Appellant's Brief at 5.) Fujimoto does not teach storing information on the DVD as the reference expressly discloses reading data from the DVD-ROM and storing graphics data in a VRAM. (*See e.g.*, Fujimoto, col. 14, ll. 9-21; Appellant's Appeal Brief at 5.) Since the Examiner's characterization is incorrect, the basis of rejection is improper. In fact, Fujimoto actually teaches that the use of a frame buffer (e.g., a large video memory) is not desirable and instead uses a smaller VRAM (i.e., smaller than a large video memory) as noted above. For these reasons in addition to those incorporated herein by reference to Appellant's Appeal Brief,

the Examiner's rejection does not constitute a *prima facie* case of obviousness and thus the claims are allowable over Fujimoto and Porter

Turning to the Examiner's statement (Examiner's Answer at 6):

> 1. a. Regarding claims 3, 7, 9, 14, 17 and 19, Fujimoto does not discourage pursuing a display system including a frame buffer that stores both video and graphics information. Fujimoto teaches not using certain areas of the VRAM 103 to improve the quality of the display without using large video memory (col. 14, ll. 9-21). Fujimoto's teaching not using large video memory is NOT directed toward the use of a single memory source, such as a DVD, to store both video and graphics data that is to be provided to the system for processing, such as scaling and mixing, before display of the combined video graphic data. Because Fujimoto does not teach eliminating the source memory that stores both the video and the graphics data he does NOT criticize using video memory to simultaneously store video and graphics data. Fujimoto's teaching does not exclude the use of video memory as a memory source for separately storing video and graphics to be supplied to a system for processing as he teaches numerous modifications and variations of his system are possible (col. 17, ll. 1-5). Additionally,

Appellant respectfully submits that, with respect to the claim language of claim 4 for example, the single frame buffer is coupled to a graphics scaler and to a video scaler while Fujimoto uses a small VRAM to store graphics data only and discourages the use of a large frame buffer for this purpose. The DVD-ROM of Fujimoto is merely read to obtain source data. Therefore the Examiner's Answer appears to be misapplying the teachings of Fujimoto. Even if the Examiner's logic were to be adopted, for argument sake, Appellant respectfully reasserts the relevant remarks from its Appeal Brief and submits that:

> [T]he substitution of a frame buffer for the DVD-ROM 100 as suggested in the Final Office Action would render VRAM 103 and main memory 13 redundant and undesirable because a frame buffer as a read/write memory would perform the same functions

> as VRAM 103 and main memory 13 with respect to graphics data 100G and video data 100B, respectively. Such a substitution would run counter to the explicit teachings found in Fujimoto. As described above, Fujimoto clearly discourages the use of a large video memory to store both graphics data 100G and video data 100B and instead eliminates it by using a dedicated graphics VRAM 103 and main memory to store encoded video. Therefore, the Examiner's suggestion creates a situation where Fujimoto teaches not to use large video memory, yet it is somehow obvious to substitute the frame buffer of Porter for the source DVD-ROM 100 of Fujimoto. (Appellant's Brief at 14.)

For this reason and for those incorporated herein by reference, there is no motivation as alleged and also Fujimoto teaches away from the substitution of a frame buffer for the source DVD-ROM 100.

As to claims 18 and 29, the Examiner's Answer characterizes Fujimoto as teaching "a multiplexer outputting graphics data to a decoder that decodes an input index value of the graphic pixel data to select a color palette address that corresponds to the graphic pixel data . . . and provides the graphic data to a scaling filter." (Examiner's Answer at 11, *describing* Fujimoto, col. 15, ll. 10-5, Figs., 1 and 17.) The Examiner's Answer concluded that "[t]hus, Fujimoto discloses a graphics decoder operably connected to the graphics scaler as he teaches decoding the graphic pixel data and providing the graphic pixel data to a filter for performing scaling operations." (Examiner's Answer at 11.)

However, Appellant's claim 18 and 29 require "a graphics decompression block operably coupled to the graphics scaler, wherein the graphics decompression block receives a compressed stream of graphics data and decompresses the compressed stream of graphics data to produce the graphics data stream" (Appellant's Brief at App. A. emphasis added), whereas the cited portion of Fujimoto teaches a known technique for color conversion – not decompression of compressed graphics data as understood by one of ordinary skill in the art in view of the specification. For instance, Fujimoto teaches that "[t]he current buffer 301 and the next buffer 302 are used for temporary storage of the graphics data read out from the VRAM 103." (Fujimoto, col. 14, l. 66 - col. 15, l. 11.) After the "multiplexer alternatively selects the current buffer 301 and next buffer 302 and outputs the graphics data in the selected buffer at the unit pixel in a serial fashion . . . the unit pixel data are supplied to the color palette 304. The color palette 304 is comprised of 256

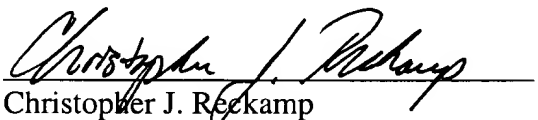
entries and an address decoder for selecting one entry amount the 256 entries by decoding an input index value of the 8 bit pixel data." (Fujimoto, col. 15, ll. 12-19.) The converted output of the color palette, YCrCb and alpha data, is subsequently sent to the current and next scaling H filters 305 and 306, respectively, and the alpha blending circuit 108. (Fujimoto, col. 15, ll. 22-23, 32-34; Figs. 1, 16 and 17.) Because the cited portion teaches color conversion and not decompression of graphics data, claims 18 and 29 are in condition for allowance.

IX. Conclusion

For the reasons advanced above, Appellant submit that the Examiner erred in rejecting pending claims 2-4, 6-11, 14, 17-23, 26-30 and 38 and in objecting to pending claims 12-13 and 24-25. Accordingly, Appellant respectfully requests reversal of the decision of the Examiner.

Respectfully submitted,

Date: October 29, 2005

By: 
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Claims on Appeal

Claim 2: The video graphics display engine of claim 4 wherein the video graphics display engine allocates a size of the first memory block of the single frame buffer and a size of the second memory block of the single frame buffer based on needs of the video data and the graphics data, respectively, and wherein the video graphics display further comprises a controller operably coupled to the video scaler and the graphics scaler, wherein the controller provides control information to the video scaler and the graphics scaler, wherein scaling operations of the video scaler and the graphics scaler utilize the control information.

Claim 3: The video graphics display engine of claim 2, wherein the merging block is operably coupled to the controller, wherein the merging block receives merging control information from the controller, wherein the merging control information is used with the scaled video stream data and the scaled graphics stream to produce the video graphics output stream.

Claim 4: A video graphics display engine comprising:

a video scaler adapted to receive a video data stream in a first format, wherein the video scaler scales video images in the video data stream based on a ratio between the video images in the first format and an output video image to produce a scaled video stream;

a graphics scaler adapted to receive a graphics data stream in a second format,

wherein the graphics scaler scales graphics images in the graphics data stream based on a ratio between the graphics images in the second format and an output graphics image to produce a scaled graphics stream;

a merging block operably coupled to the video scaler and the graphics scaler, wherein the merging block combines the scaled video stream and the scaled graphics stream to produce a video graphics output stream; and

a single frame buffer operably coupled to the graphics scaler and to the video scaler, the single frame buffer further comprises a first memory block and a second memory block, wherein the stream of video data is fetched from the first memory block and the stream of graphics data is fetched from the second memory block.

Claim 6: The display engine of claim 4, wherein the controller further comprises a video controller operably coupled to a graphics controller,

wherein the video controller is operably coupled to the video scaler, wherein the video controller provides a first portion of the control information to the video scaler,

wherein the graphics controller is operably coupled to the graphics scaler, wherein the graphics controller provides a second portion of the control information to the graphics scaler, and

wherein the video controller and the graphics controller are synchronized.

Claim 7: The display engine of claim 4, wherein the merging block performs an alpha blend operation on the scaled video stream and the scaled graphics stream to produce the video graphics output stream.

Claim 8: The display engine of claim 4 further comprises a digital to analog converter operably coupled to the merging block, wherein the digital to analog converter converts the video graphics output stream to an analog display signal.

Claim 9: The display engine of claim 4 further comprises a display driver operably coupled to the merging block, wherein the display driver is adapted to receive the video graphics output stream in digital format, wherein the display driver formats the video graphics output stream in a display compatible format.

Claim 10: The display engine of claim 4 further comprises a display driver operably coupled to the video scaler, wherein the display driver is adapted to receive the scaled video stream and produce a video display output based on the scaled video stream.

Claim 11: The display engine of claim 4 further comprises a display driver operably coupled to the graphics scaler, wherein the display driver is adapted to receive the scaled graphics stream and produce a graphics display output based on the scaled graphics stream.

Claim 12: The display engine of claim 4 further comprises a graphics flicker removal block operably coupled to the graphics scaler, wherein the graphics flicker removal block removes flicker from the scaled graphics stream.

Claim 13: The display engine of claim 4 further comprises a video flicker removal block operably coupled to the video scaler, wherein the video flicker removal block removes flicker from the scaled video stream.

Claim 14: The display engine of claim 4 further comprises a plurality of graphics scalers, wherein each of the plurality of graphics scalers receives the graphics data stream and scales the graphics images in the graphics data stream based on a ratio between the graphics images in the second format and a corresponding output graphics image to produce a corresponding scaled graphics stream.

Claim 17: The display engine of claim 4 further comprises a video decompression block operably coupled to the video scaler, wherein the video decompression block receives a compressed stream of video data and decompresses the compressed stream of video data to produce the video data stream.

Claim 18: The display engine of claim 4 further comprises a graphics decompression block operably coupled to the graphics scaler, wherein the graphics decompression block receives a compressed stream of graphics data and decompresses the compressed stream of graphics data to produce the graphics data stream.

Claim 19: The display engine of claim 4, wherein the video data stream is a decoded MPEG data stream.

Claim 20: A method for displaying video graphics data comprising:

receiving a video data stream, wherein the video data stream includes video data in a first format;

allocating a first block of a memory in a frame buffer for storing the video data stream, the allocating based upon memory needs of the video data stream;

receiving a graphics data stream, wherein the graphics data stream of includes graphics data in a second format;

allocating a second block of the memory in a frame buffer for storing the graphics data stream, the allocating based upon memory needs of the graphics data stream;

scaling the video data based on a ratio between the first format and a selected video format to produce a scaled video stream;

scaling the graphics data based on a ratio between the second format and a selected graphics format to produce a scaled graphics stream; and

merging the scaled video stream and the scaled graphics stream to produce a video graphics output stream.

Claim 21: The method of claim 20, wherein scaling the video data further comprises scaling the video data based on video data control information, and wherein scaling the graphics data further comprises scaling the graphics data based on graphics data control information.

Claim 22: The method of claim 20, wherein merging further comprises receiving merging control information, wherein the merging control information is used in merging scaled video stream am and the scaled graphics stream to produce the video graphics output stream.

Claim 23: The method of claim 20, further comprises converting the video graphics output stream to an analog format.

Claim 24: The method of claim 20, wherein scaling the video data further comprises removing the flicker from the scaled video stream.

Claim 25: The method of claim 20, wherein scaling the video data further comprises removing the flicker from the scaled graphics stream.

Claim 26: The method of claim 20, wherein scaling the video data further comprises scaling the video data based on the first format and a plurality of selected video formats to produce a plurality of scaled video streams.

Claim 27: The method of claim 20, wherein scaling the graphics data further comprises scaling the graphics data based on the first format and a plurality of selected graphics formats to produce a plurality of scaled graphics streams.

Claim 28: The method of claim 20, wherein receiving the video data stream further comprises receiving the video data stream in a compressed format, wherein the video data stream is decompressed prior to scaling.

Claim 29: The method of claim 20, wherein receiving the graphics data stream further comprises receiving the graphics data stream in a compressed format, wherein the graphics data stream is decompressed prior to scaling.

Claim 30: A video graphics integrated circuit comprising:

a frame buffer, wherein the frame buffer stores video data and graphics data;

a video scaler operably coupled to the frame buffer, wherein the video scaler scales the video data to produce a scaled video stream;

a graphics scaler operably coupled to the frame buffer, wherein the graphics scaler scales the graphics data to produce a scaled graphics stream; and

a merging block operably coupled to the video scaler and the graphics scaler, wherein the merging block combines the sealed video data stream and the graphics data stream to produce a video graphics output stream.

Claim 38: A video graphics display circuit, comprising:

a frame buffer memory maintaining video data having a first format and graphics data having a second format, wherein the frame buffer memory allocated to the video data and the graphics data is based upon memory needs of the video data and the graphics data;

a video scaler adapted to receive the video data, wherein the video scaler scales video images in the video data based on a ratio between the video images in the first format and an output video image to produce a scaled video stream;

a graphics scaler adapted to receive the graphics data, wherein the graphics scaler scales graphics images in the graphics data based on a ration between the graphics images in the second

format and an output graphics image to produce a scaled graphics stream, the video image scaling being independent of the graphics image scaling ; and

a merging block operatively coupled to the video scaler and the graphics scaler, wherein the merging block combines the scaled video stream and the scaled graphics stream to produce an video graphics output stream.

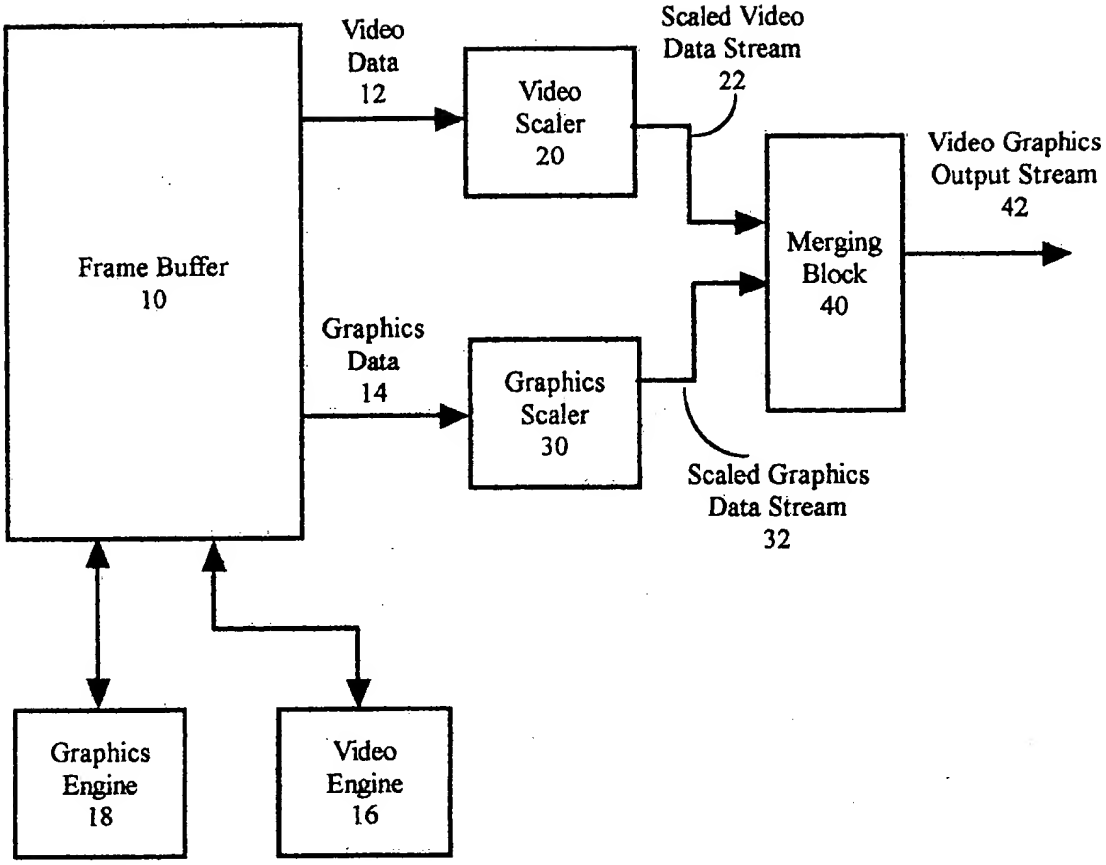

Figure 1.

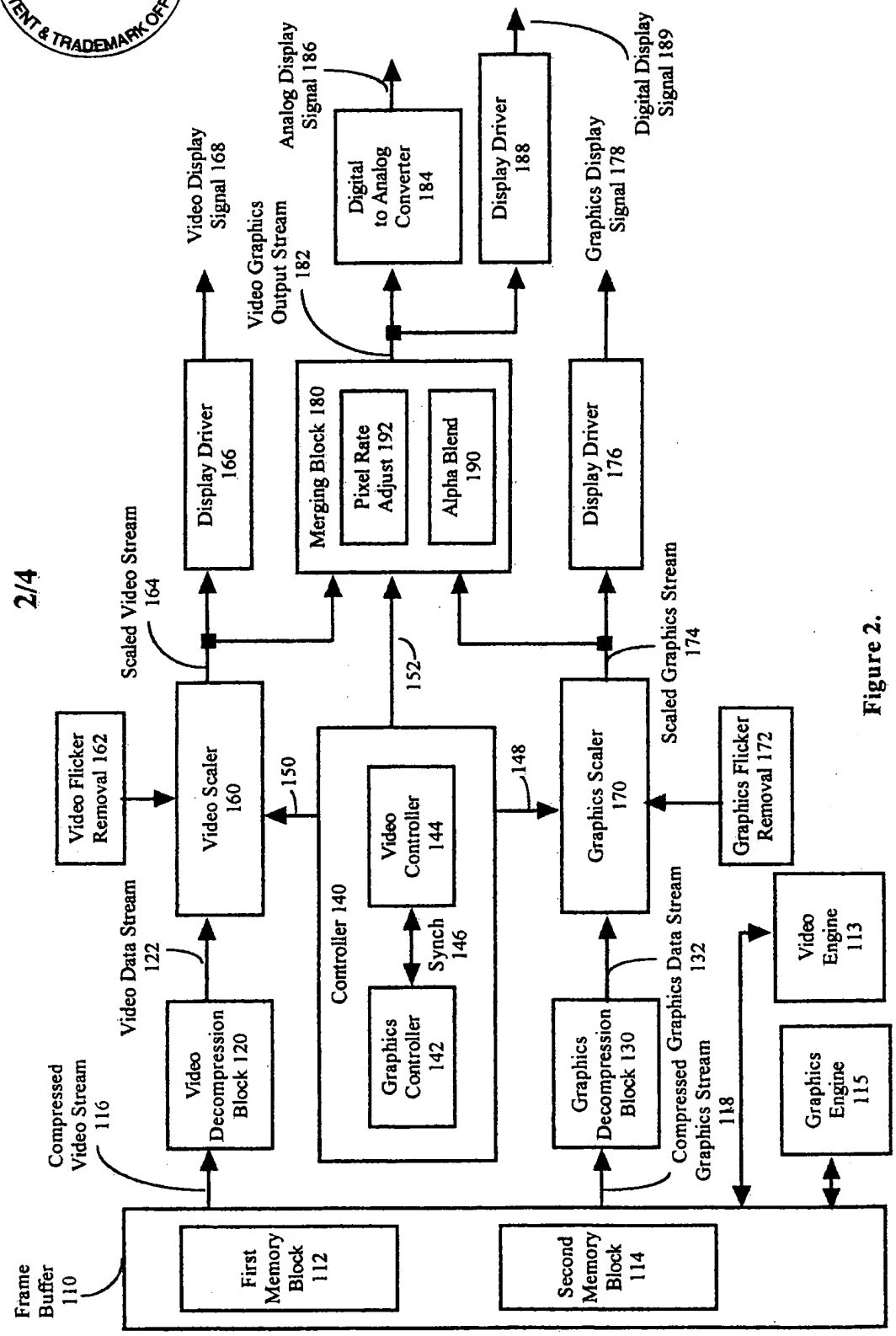

Figure 2.

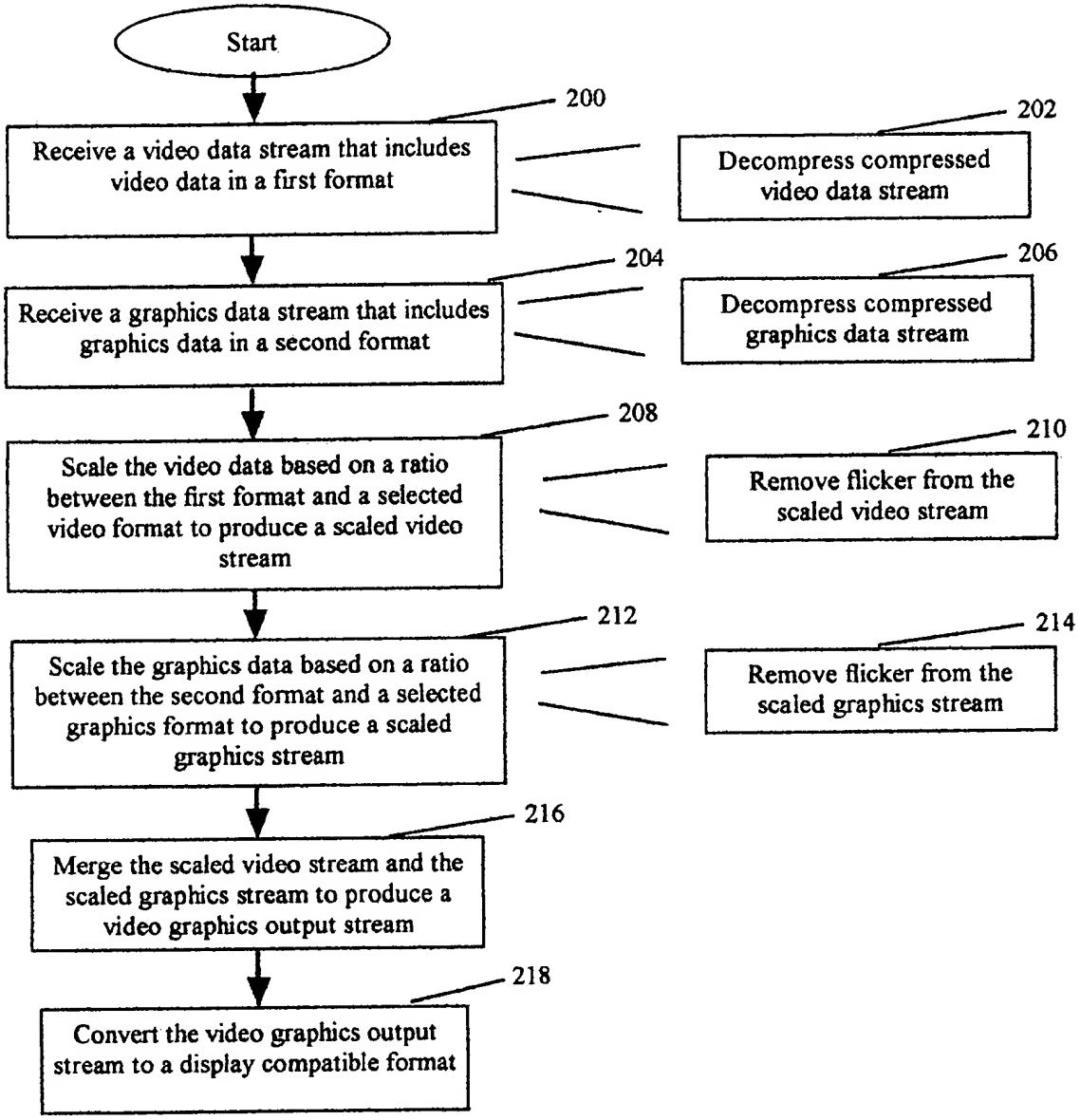

Figure 4.